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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/635,524	08/09/2000	Hiroyuki Takahashi	P19483	5635

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EXAMINER	
LEE, CHRISTOPHER E	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 10/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/635,524	TAKAHASHI, HIROYUKI	
	Examiner	Art Unit	
	Christopher E. Lee	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Receipt Acknowledgement

1. Receipt is acknowledged of the After Final Amendment filed on 26th of July 2004. Claim 1 has been amended; no claim has been canceled; and no claim has been newly added since the RCE Final Office Action was mailed on 24th of May 2004.

2. Receipt is acknowledged of the request filed on 23rd of August 2004 for a Request for Continued Examination (RCE) under 37 CFR 1.114 based on the Application No. 09/635,524, which the request is acceptable and an RCE has been established. Currently, claims 1-7 are pending in this application.

Claim Rejections - 35 USC § 103

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. Claims 1-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimada et al. [US 6,237,120 B1; hereinafter Shimada] in view of what was well known in the art, as exemplified by Crouse et al. [US 4,831,517; hereinafter Crouse].

Referring to claim 1, Shimada discloses a microcomputer (i.e., electronics apparatus in Fig. 2) including a read-only memory (i.e., ROM 15 of Fig. 2) that stores programs (i.e., firmware; See col. 3, lines 55-57 and 61-63), a controller/calculator (i.e., CPU 14 of Fig. 2) that successively accesses to addresses of said programs (i.e., firmware) stored in said read-only memory (i.e., ROM) to retrieve and decode an instruction from said accessed addresses, to execute a process based on said decoded instruction (See col. 1, lines 28-32), and a program counter (i.e., Address Controller 14 of Fig. 1, which is a part of said CPU 14 of Fig. 2) in which an address to be accessed by said controller/calculator is successively renewed, (See col. 3, lines 39-40 and col. 6, lines 41-45), said microcomputer comprising: at least one comparison-address-storage device (i.e., correcting address storing unit 3 of Fig. 1, which corresponds 16-bit interruption generating address register 21 of Fig. 2) that stores comparison address

data (i.e., correcting address) corresponding to an optional address of said programs stored in said read-only memory (i.e., address of defective portion of the firmware stored in ROM; See col. 3, lines 51-59), at which an interruption-process is executed to virtually revise (i.e., patch; See col. 3, lines 51-59) said programs stored in said read-only memory (See col. 3, lines 9-12 and col. 4, lines 23-34) by adding a program (i.e., by loading a correcting content, viz., by adding a program, into a correcting information storage means 100 in Fig. 1; See col. 3, lines 25-36); a random-access memory (i.e., RAM 26 of Fig. 2) that stores a revisional program (i.e., additional part of the program for correcting contents in ROM) in which said interruption-process is programmed (See col. 4, lines 7-9); at least one vector-address-storage device (i.e., interruption vector register 23b of Fig. 2) that stores a vector address (i.e., interruption vector) data corresponding to a head address (i.e., leading address of said correcting content stored in RAM) of said revisional program stored in said random-access memory (See col. 4, lines 35-38); and an address comparator (i.e., comparator 22 of Fig. 2) that compares said comparison address data (i.e., correcting address) with an address successively renewed in said program counter (i.e., execution address on Address Bus 16; See col. 4, lines 12-15); wherein said controller/calculator (i.e., CPU) accesses said head address of said revisional program (i.e., leading address of patch for correcting contents in RAM), stored in said random-access memory, corresponding to said vector address data stored in said vector-address-storage device (See col. 4, lines 31-34), when there is a coincidence between said comparison address data and said renewed address of said program counter (See col. 4, lines 12-17), resulting in an execution of said interruption-process in accordance with said revisional program (See col. 4, lines 31-52); a return-address-setter (i.e., ST8 and ST9 in Fig. 3B) that sets return-address data in said program counter when execution of the interruption-process in accordance with the revisional program is completed (See col. 5, lines 16-27); and an address-coincidence-disabler (i.e., switch 24 of Fig. 2) that disables said coincidence between said comparison address data and said return-address set in said program counter by said return-address-setter (i.e., the coincidence signal is disabled by the switch open; See col. 4, lines 27-34).

Shimada does not expressly teach that said return-address data coincides with said comparison address data, and said revisional program is an additional part of said programs.

The Examiner takes Official Notice that said return-address-setter that sets return-address data in said program counter to coincide with said comparison address data when execution of said interruption-process in accordance with said revisional program is completed, wherein said revisional program is an additional part of programs, is well known to one of ordinary skill in the art, as evidenced by Crouse (See Figs. 5 and 7, col. 7, line 52 through col. 8, line 36).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have coincided said return-address data with said comparison address data for adding said revisional program to said programs since it would allow that said program stored in said read-only memory (e.g., a single line of ROM code) are expanded into a larger program with said added program (i.e., multiple instructions) by means of said revisional program (i.e., a few instructions) in the patch space in said random-access memory (i.e., read-write memory), which is taught by Crouse, at col. 2, line 66 through col. 3, line 2.

Referring to claim 2, Shimada teaches a discriminator (i.e., control flag latch 23a of Fig. 2) that discriminates whether said coincidence between said comparison address data and said renewed address of said program counter is proper (See col. 4, lines 23-27; i.e., the control flag latch (discrimination system) indicates (discriminates) whether a defective portion exists within the ROM (i.e., said coincidence is proper)); and said address-coincidence-disabler (i.e., switch 24 of Fig. 2) further disables said coincidence between said comparison address data and said renewed address of said program counter (i.e., the coincidence signal is disabled by the switch open; See col. 4, lines 27-34).

Referring to claim 3, Shimada teaches a rewritable and non-volatile memory (i.e., EEPROM 27 of Fig. 2) that stores said revisional program, said comparison address data and said vector address data (See col. 4, lines 56-57); a reading/writing system (i.e., communication circuit 29 of Fig. 2) that reads said

revisional program, said comparison address data and said vector address data from said rewritable and non-volatile memory, and writes said revisional program, said comparison program, said comparison address data and said vector address data in said random-access memory (See col. 4, lines 7-9), said comparison-address-storage device and said vector-address storage device, respectively (See col. 3, line 66 through col. 4, line 11), whenever said microcomputer is powered ON (See col. 6, lines 1-7).

Referring to claim 4, Shimada teaches said address comparator (i.e., comparator 22 of Fig. 2) is connected to said program counter (i.e., Address Controller 14 of Fig. 1, which is a part of said CPU 14 of Fig. 2) to retrieve said renewed address (i.e., retrieving execution address (renewed address) on Address Bus 16, which is connected said program counter; See col. 4, lines 12-15).

Referring to claim 5, Shimada teaches said address comparator (i.e., comparator 22 of Fig. 2) is connected to an address bus (i.e., Address Bus 16 of Fig. 2) extending to said program counter (i.e., Address Controller 14 of Fig. 1, which is a part of said CPU 14 of Fig. 2), to retrieve said renewed address from said program counter (i.e., retrieving execution address (renewed address) on Address Bus 16, which is connected said program counter; See col. 4, lines 12-15).

Referring to claims 6 and 7, Shimada teaches a vector-address data setter (i.e., interruption control circuit 25 of Fig. 2) that reads said vector address data from said vector-address-storage device, and sets said vector-address-data in said program counter (See col. 3, lines 46-49, and col. 4, lines 30-34; i.e., wherein in fact that the coincidence signal input to the interruption control circuit as an interrupt request signal and the control by the CPU is moved to the address shown by an interrupt vector register by the interruption processing in the interrupt control unit implies that said vector-address data setter reads said vector address data from said vector-address-storage device, and sets said vector-address-data in said program counter), enabling access to said head address of said revisional program (i.e., leading address of patch for correcting contents in RAM) by said controller/calculator (i.e., CPU; See col. 3, lines

46-49), and execution of said interruption-process in accordance with said revisional program (See col. 4, lines 31-34).

Shimada does not expressly show a vector-address-temporary-storage device that receives said vector address data from said vector-address-storage device, when said address comparator determines that there is coincidence between said comparison address data and said renewed address of said program counter. However, Shimada further teaches said vector-address-storage device (i.e., interruption vector register 23b with 16-bits width in Fig. 2) coupled to a data bus (i.e., data bus 13 with 8-bits width in Fig. 2) is loaded into said program counter (i.e., Address Controller 14 of Fig. 1, which is a part of said CPU 14 of Fig. 2) coupled to an address bus (i.e., Address Bus 16 with 16-bits width in Fig. 2). Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have included said vector-address-temporary-storage device in said controller/calculator (i.e., CPU 14 of Fig. 2), which receives said vector-address data from said vector-address-storage device, when said address comparator determines that there is said coincidence between said comparison address data and said renewed address of said program counter (i.e., when the interrupt occurs) since said data bus (8-bits width) cannot support a direct transfer (viz., single transferring transaction) of said vector address data (16-bits width) from said vector-address-storage device (16-bits width) to said program counter (16-bits width) without said vector-address-temporary-storage device, which could be temporarily holding (viz., buffering) and assembling two 8-bits width said vector-address data into a single 16-bits width said vector-address data for said 16-bits width said program counter and its coupled address bus.

Therefore, Shimada inherently suggests said vector-address data setter (i.e., interruption control circuit 25 of Fig. 2) that reads said vector address data from said vector-address-temporary-storage device, and sets said vector-address-data in said program counter (See col. 4, lines 30-34; i.e., wherein in fact that the coincidence signal input to the interruption control circuit as an interrupt request signal and the control by the CPU is moved to the address shown by an interrupt vector register by the interruption processing in

the interrupt control unit implies that said vector-address data setting system reads said vector address data from said vector-address-temporary-storage device, and sets said vector-address-data in said program counter).

Response to Arguments

5. Applicant's arguments filed on 26th of July 2004 have been fully considered but they are not persuasive.

In response to the Applicant's argument with respect to "... Thus, SHIMADA does not disclose, inter alia, a return address setter that sets a return address that coincides with the comparison address data and does not return the address at least because the address is abolished. Additionally, SHIMADA does not disclose an address-coincidence-disabler because SHIMADA merely jumps to another portion of the program and has no need to disable in the manner recited in claim 1." on the Response page 8, lines 3-12, the Examiner respectfully disagrees.

Shimada teaches that ST8 and ST9 in Fig. 3B (i.e., return address setter) that sets return address data in a program counter when execution of an interruption-process in accordance with a revisional program is completed (See col. 5, lines 16-27) with the exception of said return-address data coinciding with a comparison address data. However, the claimed limitation "a return-address-setter that sets return-address data in the program counter to coincide with the comparison address data when execution of said interruption-process in accordance with the revisional program is completed" is well known to one of ordinary skill in the art, as evidenced by Crouse (See Crouse, Figs. 5 and 7, col. 7, line 52 through col. 8, line 36). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have coincided said return-address data with said comparison address data for adding said revisional program to said programs for the advantage of allowing that said program stored in said read-only memory (e.g., a single line of ROM code) are expanded into a larger program with said added program (i.e., multiple instructions) by means of said revisional program (i.e., a few instructions) in

the patch space in said random-access memory (i.e., read-write memory), which is taught by Crouse, at col. 2, line 66 through col. 3, line 2.

And, in contrary to the Applicant's statement, Shimada teaches a switch 24 (i.e., address-coincidence-disabler) in Fig. 2 that disables a coincidence signal (i.e., coincidence) between a correcting address (i.e., comparison address data) and return-address set in a program counter by the steps ST8 and ST9 in Fig. 3B (i.e., return-address-setter; See col. 4, lines 27-34). Actually, Shimada clearly suggests the claimed subject matter "coincidence", i.e., coincidence signal, is disabled by the claimed subject matter "address-coincidence-disabler", i.e., switch, open, for enabling/disabling the claimed subject matter "virtually revising" based on the indication whether or not a defective portion exists within the ROM 15 in Fig. 2 (See col. 4, lines 23-24), instead of merely jumping to another portion of a program.

Refer to paragraph 4 of the instant Office Action, claims 1-7 rejection under 35 U.S.C. 103(a) as being unpatentable over Shimada in view of what was well known in the art, as exemplified by Crouse.

Thus, the Applicant's argument on this point is not persuasive.

In response to the Applicant's argument with respect to "CROUSE discloses an insertion point 36 that executes additional code 38. After the additional code is executed, a RWM branch instruction 39 provides an address for a ROM instruction immediately after insertion point 36. In this regard, CROUSE does not disclose a return-address-setter that sets an address to coincide with the comparison address data. Instead, CROUSE stores an instruction for a subsequent address. Additionally, CROUSE does not have an address-coincidence-disabler because CROUSE jumps to a subsequent address and thus also has no need to disable, as recited in claim 1." on the Response page 8, lines 13-20, the Examiner believes that the Applicant misinterprets the claim rejection.

The Applicant essentially argues that Crouse doesn't teach the above argued elements. However, Shimada teaches the claimed subject matters "return-address-setter" and "address-coincidence-disabler", and Shimada in view of what was well known in the art, as exemplified by Crouse, suggests all the limitations

recited in the claim 1 (See paragraph 4 of the instant Office Action, claims 1-7 rejection under 35 U.S.C. 103(a) as being unpatentable over Shimada in view of what was well known in the art, as exemplified by Crouse).

Thus, the Applicant's argument on this point is not persuasive.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher E. Lee whose telephone number is 703-305-5950. The examiner can normally be reached on 9:30am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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